Extending the Constant Power Speed Range of the Brushless DC Motor Through Dual-Mode Inverter Control

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Abstract—An inverter topology and control scheme has been developed and tested to demonstrate that it can drive low-inductance, surface mounted permanent magnet motors over the wide constant power speed range (CPSR) required in electric vehicle applications. This new controller, called the dual-mode inverter controller (DMIC) [1], can drive both the Permanent Magnet Synchronous Machine with sinusoidal back emf, and the brushless dc machine (BDCM) with trapezoidal emf as a motor or generator. Here we concentrate on the application of the DMIC to the operation of the BDCM in the motoring mode. Simulation results, supported by closed form analytical expressions, show that the CPSR of the DMIC driven BDCM is infinite when all of the motor and inverter loss mechanisms are neglected. The expressions further show that the ratio of high-to-low motor inductances accommodated by the DMIC is 11 making the DMIC compatible with both low- and high-inductance BDCMs. Classical hysteresis-band motor current control used below base speed is integrated with DMICs phase advance above base speed. The power performance of the DMIC is then simulated across the entire speed range. Laboratory testing of a low-inductance, 7.5-hp BDCM driven by the DMIC demonstrated a CPSR above 6:1. Current peak and rms values remained controlled below rated values at all speeds. A computer simulation accurately reproduced the results of lab testing showing that the limiting CPSR of the test motor is 8:1.

Index Terms—Brushless dc machine (BDCM), constant power speed range (CPSR), dual-mode inverter controller (DMIC).

I. THEORY AND SIMULATION

THE TRAPEZOIDAL back emf brushless dc motor (BDCM) with surface-mounted magnets has high power density and efficiency especially when rare-earth magnet materials such as samarium-cobalt or neodymium-iron-boron are used. Traction applications, such as electric vehicles, could benefit significantly from the use of such motors. Transmissionless electric passenger vehicles require a constant power speed ratio (CPSR) of 4:1 or more. Larger electric vehicles, such as heavy trucks, tanks, and other heavy equipment, can require a CPSR of 10:1. Unfortunately, a practical means for driving the BDCM over a CPSR of 4:1 to 6:1 has not been demonstrated. A key feature of these motors is that they have low internal inductance. Conventional phase advance (CPA) methods [2]–[5] are effective in controlling the motor power over such a speed range. However, the current at high speed may be several times greater than that required at the base speed. The increase in current during high-speed operation is caused by the low motor inductance and the action of the bypass diodes of the inverter [6], [7]. The use of CPA with a low-inductance motor requires an increased current rating of the inverter semiconductors and additional cooling. Added cooling would be required for the inverter, where the losses increase proportionally with current, and for the motor, where the losses increase with the square of the current. As suggested for the sinusoidal emf motor [8], external series inductance can be added to mitigate the high-current problems associated with CPA. However, this reduces power density, could require an increase in supply voltage, and leaves the CPSR performance of the system highly sensitive to variations in the available voltage. A new inverter topology and control scheme has been developed that can drive low-inductance BDCMs over the CPSR that would be required in electric vehicle applications [1]. This new controller is called the dual-mode inverter control (DMIC).

The DMIC has the following features.

1) Internal motor inductance can be low and is not a critical parameter. Analytical results show that an inductance range of at least 11:1 can be tolerated.

2) Independent of speed, the motor current can be controlled to remain within the rated rms value over the extended CPSR. Using the DMIC does not increase motor-cooling requirements or increase the current-handling requirement of inverter-switching components.

3) The DMIC works with either the Permanent Magnet Synchronous Machine (PMSM) with sinusoidal back emf [9] or the BDCM with trapezoidal back emf.

4) Motoring and regeneration can be controlled. For a low-inductance motor, it can be possible to regenerate at several times rated power for brief periods. This feature is attractive for applications requiring rapid regenerative braking.

5) For high-inductance motors, up to 50% more power can be developed during high-speed motoring operation than can be developed at base speed at the same rms motor current. The exact amount of additional power depends on the inductance.
6) The controller provides the functional equivalent of field weakening without requiring an auxiliary field winding and its necessary controls or rotor saliency.

CPA uses the common six-transistor, voltage source inverter (VSI) topology. The DMIC supplements the common VSI with six thyristors, which, in addition to enabling the performance enhancements, provide several important failure mode protection features. These features are especially important in electric vehicle applications and include the following.

1) The DMIC inverter is capable of isolating the permanent magnet motor from short circuits that might develop in the dc supply system or in the inverter transistors.
2) A controller board failure with the DMIC and attendant loss of semiconductor firing signals results in rapid extinction of motor current so that the vehicle simply coasts. This same failure with CPA and the common VSI results in heavy regenerative braking.
3) The DMIC inverter transistors can be rated for the dc supply voltage. High-voltage blocking, under normal or abnormal conditions, is handled by the thyristors.

II. THEORETICAL HIGH-SPEED DMIC PERFORMANCE

In Section I we concentrate on the high-speed performance of the DMIC in the motoring mode. Generating/braking operation for the BDCM is discussed in [6] while the application of the DMIC to high speed operation of the sinusoidal back emf machine can be found in [9].

A. DMIC Inverter Topology and Semiconductor Firing Scheme

The DMIC inverter topology and permanent magnet motor model used in this work are shown in Fig. 1. The inverter consists of a common six transistor VSI bridge, each transistor having a parallel bypass diode. The bridge is interfaced to the motor through an ac voltage controller, which consists of three pairs of antiparallel silicon controlled rectifiers (SCRs). A detailed discussion of the operation of the inverter can be found in [3], consequently, only a brief discussion is given here.

The purpose of the thyristors is to block undesired conduction of the bypass diodes during high-speed operation. During high-speed motoring, the magnitude of the motor emf is substantially larger than the value of dc supply voltage. Since the bypass diodes form a diode rectifier between the high-voltage source of the motor emf and the dc supply, there is a natural tendency toward regeneration when the common VSI is used. In the DMIC inverter, motor current normally flows through the series combination of a transistor and a thyristor although during commutation the current flow may be through a bypass diode and a thyristor. Since the thyristor will not reverse conduct, the current is shut off at the current zero crossing. In previous work [6], [7] it was shown that high-speed operation is a mixture of motoring and regeneration when phase advance is applied using the common VSI. For low-inductance motors, the current at high speed with CPA may be several times greater than the motor base speed rating and the mixture of motoring and regeneration is extreme. The regeneration is associated with conduction of the bypass diodes, while the motoring component is associated with conduction of the transistors. The braking component is large and cancels a like portion of the motoring component, leaving a modest net motoring component. In the DMIC, the thyristors, which will not reverse conduct, eliminate the braking component that would otherwise result from bypass diode conduction. The elimination of the braking component allows rated power to be developed at a greatly reduced current level. Despite the additional voltage drops associated with the thyristors, the efficiency of the DMIC drive is superior to that of CPA when the motor inductance is low.

In addition to remaining within current rating during high-speed operation at rated power, thyristor control provides several fault tolerance benefits already mentioned.

The firing commands for the semiconductors in phase a, transistors, Q1 and Q4, and thyristors, T1 and T4, are shown in Fig. 2. The firing commands for phases b and c are analogous to those for Fig. 2 but are delayed by one-third and two-thirds of a cycle, respectively. Below base speed, the BDCM operates on two phases at a time in a “single phase” mode. Except for a short commutation overlap period, the supply current flows into the motor through one phase and returns through a second phase, while the third phase idles. Because of the tendency of bypass diodes to conduct at high speed, the single-phase mode of operation is lost when CPA is used with the common VSI. In the CPA, the motor phase currents become continuous and...
no phase ever idles. Because of the thyristors, the DMIC is able to extend the single-phase operation to speeds above base speed. The term “dual-mode inverter control” refers to the fact that below base speed the motor current is controlled via hysteresis band pulse width modulation (PWM) regulation, which involves high-frequency switching, while above base speed the motor current is controlled by the fundamental frequency phase advance switching pattern shown in Fig. 2. The thyristors of the DMIC do not interfere with the PWM regulation below base speed and are fired at the fundamental frequency regardless of motor speed. The commutation of the thyristors is natural, taking place at phase current zero crossings so that commutation circuitry is not required.

In Fig. 2 $\Theta_a$ is the “advance angle.” The advance angle is measured projecting backward in time from the instant at which the line-to-line back emf, $e_{ab}$, equals the supply voltage, $V_{dc}$. For transistor Q1 and thyristor T1 the relevant intersection is marked as point “A” in the figure while for transistor Q4 and thyristor T4 the relevant intersection is point B in the figure. The advance angle has a range of 0 to 60°. The dwell angle of the transistors is noted as $180^\circ - \Theta_b$, where $\Theta_b$ is the “blanking angle,” which provides a safety precaution in conventional inverters against short circuits of the dc power supply. Beginning at base speed, and continuing to about 1.5 times base speed, the blanking angle is progressively reduced from 60 to 0°. This has been shown to maximize motoring power per rms amp of motor current at high speed. In the high speed generating/braking mode, the transistors are not fired and the thyristors, T1 and T4, are fired at an advance angle, $\Theta_{\alpha}$, relative to the intersections marked at points A’ and B’, respectively in Fig. 2. Further details on regenerative braking are in [6].

The six thyristors used in the DMIC inverter clearly represent additional cost beyond the standard VSI configuration. When the motor inductance is low, inductance values are quantified below, the added cost of the thyristors must be weighed against the accommodation that must be reached to use the standard VSI inverter and the CPA control method. These accommodations may include increased current rating of the inverter components and added cooling system load for both motor and inverter, external inline inductors and higher dc supply voltage, or redesign of the BDCM for a higher inductance along with added dc supply voltage, or derating an oversized motor and inverter. There are also the enhanced reliability and fault tolerance features of the DMIC to consider. The authors are presently engaged in a project to investigate these tradeoffs in a commercial application.

The parameters of the BDCM are defined and values used for the theoretical calculations in Section I and the test calculations in Section III are summarized in Table I. The values represent a motor designed by ORNL and used for the proof-of-principle lab demonstration of a 6:1 CPSR described in Section III.

The 188.7-V supply is the voltage required by the motor to develop rated torque at the base speed of 2600 rpm when winding resistance is included. In the simulations discussed in this paper the inverter voltage drops are neglected.

The values for $I_{pk}$ and $I_{trms}$ assume the classical idealized rectangular phase current wave shape that typifies the ideal operation of the BDCM below base speeds and has a rectangular shape of 120° duration each half cycle. $I_{pk}$ and $I_{trms}$ will be used as current ratings for the simulated performance.

The example motor was not built for high-speed operation, and the capability of its rotor to survive speeds above 3000 rpm is not known. However, in this study, the performance of the motor is simulated for speeds of six times base speed (15 600 rpm). Rotor designs for high-speed operation are under development, and a full-scale test of the DMIC on a motor capable of high speed will be conducted in the future. In the short term, the example motor has been operated in the laboratory using the DMIC control at reduced dc supply voltage, which effectively reduces the base speed and the power rating of the...
B. Simulated Performance Neglecting Losses

MATLAB and PSPICE simulations have been developed for implementing the motor model and the switching actions of the inverter and control scheme. In this section, we consider simulation of the DMIC in the motoring mode, neglecting all loss mechanisms including winding resistance, friction, windage, hysteresis, and eddy currents. The inverter semiconductors are modeled as ideal devices.

Concepts such as base speed and CPSR can be defined in different ways. In this work, base speed is the highest speed at which rated torque can be developed in the low-speed current regulation mode. Rated power is then the power developed at base speed and rated torque. The CPSR is the ratio of the highest speed at which rated power can be developed while operating within the current rating, divided by the base speed.

With no resistive losses, a dc supply voltage of 183.4 V is required to establish a base speed of 2600 rpm for the example motor. Fig. 3 displays the instantaneous phase A motor current and instantaneous total output power over one fundamental electrical cycle at a relative speed of 7800 rpm for advance angles of 20°, 30°, and 40°. The simulator also calculates performance measures such as peak and rms motor current and average power also recorded in Fig. 3. For advance angles below 30°, the current waveform is simply scaled in time but is otherwise unchanged. This is an important feature of a controller that provides an infinite CPSR. In CPA, the current magnitude for a given advance angle increases with speed, thereby limiting the CPSR. Also note, again by comparing Figs. 4 and 3, that the average developed power depends on advance angle but not on speed. Although average power with DMIC depends on advance angle, but not speed, the power ripple increases with speed.

The power produced by the DMIC is not smooth but contains ripple at six times fundamental electrical frequency. In electric vehicle applications, the equivalent inertia of the vehicle will provide sufficient filtering such that torque pulsations will not offend the vehicle operator. The rms current at 40° advance is 184.4 A, which is less than the 202.3-A rating, yet the average power is 42.34 kW, which exceeds the 36.93 kW that can be developed at base speed. Although not shown here, an advance angle of 41.2° results in rated rms current and the power produced is 46.76 kW, which is almost 27% more than rated. It is typical of the DMIC that, once the speed is high enough for the blanking angle to be reduced to zero, more power is developed than is developed at base speed. Similar results are observed with CPA [3].

Fig. 4 repeats the simulations of Fig. 3 for the relative motor speed, 7800 rpm (n = 3) and $V_{dc} = 183.4$ V.

### Table I

<table>
<thead>
<tr>
<th>Definition</th>
<th>Value for ORNL BDCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p$</td>
<td>number of poles</td>
</tr>
<tr>
<td>$N_s$</td>
<td>base speed rpm</td>
</tr>
<tr>
<td>$\phi_s$</td>
<td>base speed electrical rad/sec</td>
</tr>
<tr>
<td>$I_{[A]}$</td>
<td>peak current</td>
</tr>
<tr>
<td>$I_{[B]}$</td>
<td>rated output power, kW</td>
</tr>
<tr>
<td>$T_e$</td>
<td>rated output torque</td>
</tr>
<tr>
<td>$I_{[C]}$</td>
<td>self inductance per phase</td>
</tr>
<tr>
<td>$L_{[D]}$</td>
<td>leakage inductance per phase</td>
</tr>
<tr>
<td>$M$</td>
<td>mutual inductance</td>
</tr>
<tr>
<td>$L_1$</td>
<td>equivalent inductance per phase</td>
</tr>
<tr>
<td>$R$</td>
<td>winding resistance, ohms per phase</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>dc supply voltage</td>
</tr>
<tr>
<td>$\varphi_a$</td>
<td>phase a to neutral voltage</td>
</tr>
<tr>
<td>$\varphi_b$</td>
<td>phase a to neutral back emf</td>
</tr>
<tr>
<td>$\varphi_c$</td>
<td>phase a to phase b back emf</td>
</tr>
<tr>
<td>$N$</td>
<td>actual motor speed rpm</td>
</tr>
<tr>
<td>$n$</td>
<td>relative rotor speed</td>
</tr>
<tr>
<td>$E_{[A]}(n)$</td>
<td>peak phase-to-neutral emf at speed n, V</td>
</tr>
<tr>
<td>$E_{[B]}(n)$</td>
<td>peak phase-to-phase emf at speed n, V</td>
</tr>
</tbody>
</table>

1. Does not include inverter voltage drop.
2. Value is 183.4 V if winding resistance is neglected.
3. Includes inverter voltage drop of 0.3 V.
Fig. 4. Instantaneous phase a motor current and power at 15 600 rpm (n = 6) and V solicit = 183.4 V.

Fig. 5. Instantaneous phase a motor current and power at 15 600 rpm (n = 7.32) and V solicit = 150 V.

Fig. 6. Average power and current versus advance angle at 7800 and 15 600 rpm for V solicit = 183.4 V (n = 3 and n = 6) and V solicit = 150 V (n = 3.66 and n = 7.32) for L = 73.6 μH.

Fig. 6 graphically confirms that the DMIC is an infinite CPSR control in the absence of losses. The time domain simulator was used to calculate rms current and average power as the advance angle changed from 0° to 60° in steps of 3°. Runs were made for two supply voltages, 183.4 and 150 V, and for two speeds, 7800 and 15 600 rpm. Thus, there are a total of four operating conditions. Note that in Fig. 6 there appears to be a single trace of rms current versus advance angle. Actually, there are four traces lying on top of one another; rms current varies with advance angle but not with speed or supply voltage. Also in Fig. 6, there appears to be two traces of average power versus advance angle. Again, there are actually four plots. Average power depends on advance angle and supply voltage but not on speed. Fig. 6 also shows that the DMIC controls power and current concurrently. That is, the greater the advance angle, the greater the rms current, and thus the greater the power developed. This is in contrast to CPA, where the advance angle controlled the power but the useful current was relatively constant with variation in advance angle. In the DMIC, the rms current at zero output power is zero. Thus, the copper losses during “coasting” are zero, unlike CPA where the copper losses are virtually independent of output [7].

C. Motor Control With DMIC

Below base speed, the DMIC controls the motor using the usual hysteresis band current regulator. Using our definition, base speed is the highest speed at which rated torque can be achieved by the current regulator. Beginning at base speed, and for all higher speeds, the phase must be advanced to sustain current flow into the motor. It is also desirable to reduce the blanking angle from 60° toward zero. We have found that for low-inductance motors, the blanking angle can be reduced over a speed range of n = 1 to n = 1.6, while for higher induc-
tance motors a larger interval is appropriate to avoid commutation failures.

Fig. 7 shows a simple strategy for combining the low-speed current regulation control with the high-speed phase advance. This figure was generated over a speed range from a few hundred to 15 600 rpm \((n = 6)\) with the time domain simulator, which includes models of the current regulator and phase advance. The figure shows the activity in the control channels, the rms current, and the average power as functions of motor rpm. The control signals are the current regulator set point, Isat, advance angle, \(\theta_a\), denoted as “tha” in the figure, and blanking angle, \(\theta_b\), denoted as “thb” in the figure. At each speed, the control parameters were adjusted to yield rated rms current, 203.3 A, to display the maximum power versus speed capability of the DMIC.

Fig. 7 was constructed for the nominal motor parameters, \(L = 73.6 \mu H\) and \(V_{dc} = 183.4 V\). The base speed for this case is 2600 rpm, which corresponds to the onset of activity in the advance regulator control channel. At base speed and rated current, the power produced is the rated value, 36.9 kW. This value is marked as a reference in the figure. Note that the power produced at speeds above base speed is greater than the rated power. The power at high speed is 46.7 kW.

### D. Theoretical Performance Neglecting Losses

When losses are neglected, the differential equations describing the DMIC inverter/BDCM have been solved analytically and closed-form expressions for peak motor current, rms current, and average power have been derived. A detailed derivation can be found in [6]. In this section, we extract the expressions for peak and rms current and rms power, which complement the simulation results of the previous section.

For relative speed greater than or equal to 2 and for advance angles of 30 to 60° these performance metrics are (1)–(3) shown at the bottom of the page.

Advance angle, \(\theta_a\), in these expressions is in electrical radians rather than degrees. These expressions explain several observations made based on the simulated results of the previous section. Observe that the peak and rms values of current do not depend on the values of dc supply voltage or motor speed with the restrictions noted previously. In the more detailed reference [6], it is shown that the time domain expressions for phase current are also independent of \(V_{dc}\) and relative speed, \(n\). As motor speed increases for a fixed advance angle, the current waveform simply compresses in time, corresponding to the increase in electrical frequency. Also note that the average power is independent of speed and scales linearly with supply voltage. These results confirm that the DMIC provides an infinite CPSR when all loss factors are neglected.

Expression (2) for rms current provides a way to bracket the inductance needed by DMIC. Setting \(\theta_a\) equal to 30° (0.5235 rad), which is the critical advance angle for continuous conduction, and solving for \(L\) yields a minimum inductance condition

\[
L_{\text{min}} = \frac{\pi E_d}{\Omega h i_b \sqrt{1020}}.
\]

Setting \(\theta_a\) equal to 60° (1.047 rad) and solving (2) for \(L\) yields a maximum inductance condition

\[
L_{\text{max}} = \frac{\pi E_d}{\Omega h i_b \sqrt{91215}}.
\]

Note that the ratio of \(L_{\text{max}}\) to \(L_{\text{min}}\) is 11.0, independent of motor parameters, and exceeds one order of magnitude.

The implication here is that in a given application the motor designer can optimize the motor design based on machine considerations and that the DMIC will be able to drive the resulting

\[
I_{pk} = \max \left\{ \frac{E_d}{\Omega h i_b} \left[ \frac{\theta_a}{3} - \frac{5\pi \theta_a^3}{18} + \frac{2\pi \theta_a^5}{15} \right] \right\} \tag{1}
\]

\[
I_{\text{rms}} = \frac{E_d}{\Omega h L} \left\{ \frac{1}{\pi} \frac{8}{5\pi^2} \theta_a^5 + \frac{8}{3\pi} \theta_a^4 + \frac{16}{9} \theta_a^3 + \frac{4\pi}{27} \theta_a^2 - \frac{16\pi^2}{81} \theta_a + \frac{23\pi^3}{1215} \right\} \tag{2}
\]

and

\[
P_{\text{avg}} = \frac{2V_{dc} E_d}{\pi^2 h L} \left\{ \theta_a^3 + \pi \theta_a^2 + \frac{\pi^2}{3} \theta_a - \frac{2\pi^3}{27} \right\} \tag{3}
\]
motor within its current rating. Although all of the above formulas are based on zero winding resistance, they give good results even when R is not zero.

Applying (4) and (5) to the example motor results in

$$I_{\text{min}} = 17.4 \mu \text{H}$$
$$I_{\text{max}} = 192 \mu \text{H}$$

The example motor inductance is 73.6 \(\mu\text{H}\) and the previous results show that this value could be significantly reduced or increased without impacting the DMICs ability to provide rated power at high speed while remaining within the rms current limit.

Fig. 8 shows the variation of rms current and average power versus advance angle at six times base speed for inductance values of one half and two times that of the example motor, 36.8 \(\mu\text{H}\) and 147.2 \(\mu\text{H}\). In each case, the supply voltage was adjusted to keep base speed at 2600 rpm. The low-inductance motor required only 166.5 V as compared to the nominal value of 183.4 V while the high-inductance motor required 216.8 V. The curves in Fig. 8 were generated using the lossless simulator. Fig. 8 shows the instantaneous phase currents and instantaneous power developed at 15 600 rpm for the two inductance cases with the advance angle adjusted in each case to result in rated current. At the rated current of 202.3 A, the low-inductance motor delivers 40.79 kW while the high-inductance motor delivers 57.65 kW. When winding resistance is included, the high-inductance motor would have the greater efficiency, more watts per rms amp. However, the higher inductance requires a much higher dc supply voltage to sustain the base speed of 2600 rpm and has substantially reduced peak power capability.

### III. Laboratory Proof-of-Principle

In previous work we have shown that when all drive loss mechanisms are neglected the CPSR of the BDCM is infinite when driven by the DMIC [6]. Losses are unavoidable in a physical drive and will limit the CPSR to a finite value. Speed dependent losses such as skin effect in winding resistance, hysteresis and eddy currents, and friction and windage consume progressively more input power as speed increases; consequently, the extent of the CPSR is limited by the speed-dependent losses when the motor current is constrained to its rating. In this work we report laboratory test results for a low-inductance, 7.5-hp BDCM driven by the DMIC. Dynamometer measurements show that the CPSR is greater than 6:1. The speed rating of the test machine precluded evaluation at higher speeds. Test results show that the motor current waveform, peak, and rms values remain under control as speed increases.

The laboratory testing allowed quantification of the important speed-sensitive losses of the test motor. These losses were incorporated into simulation models of the DMIC. Simulation results, including the loss effects, are shown to agree with test measurements. Current waveform shape, rms current, and useful output power of the model match the experimental results. The model is then used to show that the CPSR of the test motor is 8:1.

The test motor was not designed to be operated with the DMIC over a wide speed range. For example, the stator laminations are 14 mils thick. The core losses of the motor can be reduced, and the CPSR extended, by using thinner laminations.

#### A. Test Hardware

The test motor, whose parameters are summarized in Table I, is a 12-pole, axial gap, 2600 rpm, 49.5-hp, 220-V motor with neodymium-iron-boron magnets.

This motor was not designed for operation significantly above 2600 rpm. To demonstrate the broad CPSR capability of the DMIC, and remain within the safe speed rating of the rotor, testing was conducted with reduced supply voltage. This effectively reduces the base speed of the motor and lowers the power rating. A base speed of 400 rpm was chosen so that a CPSR of 6:1 could be safely demonstrated on the test machine.

Running on a 220 Vdc supply, the efficiency of the example motor is approximately 94% at rated conditions. Under the reduced voltage/power output conditions of this test, the motor efficiency will be around 70% at base speed and above since the losses are those of a 49.5 hp motor while the power output is reduced to 7.5 hp. We will not dwell on efficiency calculations in this work since its purpose is to confirm the broad CPSR capability of the DMIC. A motor specifically designed for operation with the DMIC has been built and will be tested at a later time to provide a more accurate picture of the efficiency.

The dc supply voltage is a key parameter affecting the base speed of the motor. An accurate test of the motor CPSR cannot be conducted if the supply voltage is larger than the minimum necessary to supply rated torque at the specified base speed. To establish a base speed of no more than 400 rpm, the motor was tested in the laboratory with the current regulator disabled and...
Fig. 9. Measured rotational losses versus rotor speed for the test motor.

the phase advance set to about 30°. The dc supply voltage was slowly increased until at 41.9 V, the output power measured by the dynamometer equaled 7.5 hp at 400 rpm. This ensured that the supply voltage is less than what would be required in the current regulation mode to support a base speed of 400 rpm. The measured motor rms current at this condition was 212 A, and this was accepted as the current rating of the motor while rated power is 7.5 hp. Even though the true base speed of the test setup is less than 400 rpm, we will use 400 rpm as “the” base speed and our conclusions about the CPSR range of the DMIC will be understated.

The aggregate of the speed-sensitive core and rotational losses can be measured easily using a dynamometer to drive the de-energized motor. For convenience, the aggregate of these losses is referred to simply as rotational losses. A plot of measured total rotational losses versus rotor speed is shown in Fig. 9.

In addition to skin effect changes, the winding resistance is sensitive to winding temperature. To characterize winding resistance, the laboratory setup included measurement of the total three-phase power entering the motor and rms motor current. When operating near rated rms motor current, the output power measured by the dynamometer plus the appropriate rotational losses from Fig. 9 can be subtracted from the measured total input power to the motor to determine the total copper loss. Dividing the copper loss by three and by the square of the rms motor current yields the per-phase winding resistance appropriate for rated current and the speed at which the measurements are made. Test data for the example motor when operating near rated current for speeds of 400, 1215, and 2424 rpm were used to construct the winding resistance versus speed plot shown in Fig. 10.

The curve of Fig. 10 is a straight line, and for the rotor speed of N (in rpm) the motor winding resistance is given by

\[ R = 0.01423 + 1.433 \cdot 10^{-6} \cdot N \Omega \text{ per phase.} \]  

Fig. 10. Winding resistance versus rotor speed for operation at rated current, calculated from measurements at 400, 1215, and 2424 rpm.

of operation. However, long cables were used to connect the DMIC inverter to the motor, the net effect of which was an equivalent inductance increased to 94 \( \mu \)H per phase.

Inverter semiconductor switching frequency during high-speed operation of the DMIC is at the fundamental electrical rate. This rate was 240 Hz, or less, during the testing of the example motor, and inverter switching losses are small. Conduction losses are important because they reduce the supply voltage available at the terminals of the motor. During testing, the line-to-line voltage at the motor terminals was observed using an oscilloscope. It was observed that of the 41.9 V at the dc supply, only 33.6 V was available to the motor. When testing at the 212-A rms current rating, the value of 33.6 V was consistently observed regardless of the motor speed. In our MATLAB and PSPICE simulators, the inverter switching logic of transistors, diodes, and thyristors are represented in detail. However, the devices are modeled as ideal elements. Consequently, in the simulators, the equivalent value of 33.6 Vdc rather than the 41.9 V of the actual supply, represents the supply voltage.

B. DMIC Inverter Topology, Firing Scheme, and Motor Model

The DMIC inverter topology and motor model used in this work appear in Fig. 1. The DMIC firing scheme for the phase a semiconductors during high-speed motoring operation are shown in Fig. 2. The firing logic for phases b and c are analogous to that of phase a with delays of one third and two thirds of a cycle, respectively. Detailed rationale behind the inverter topology and its firing scheme can be found in companion work [6].

The parameter, \( R_{rot} \), in Fig. 1, is an equivalent resistance representing the aggregate rotational losses of the motor. Since the rotational losses vary with speed, as shown in Fig. 9, the value of \( R_{rot} \) changes with rotor rpm. The phase-to-neutral back emfs are trapezoids with the rms value at relative rotor speed, \( n \), given by

\[ V_{rms} = n F_b \sqrt{\frac{7}{9}} \text{ volts.} \]
Combining this with a point from the rotational loss curve of Fig. 9, the value of $R_{rot}$ can be calculated for a given speed as

$$R_{rot} = \frac{3V_{rms}^2}{P_{rms}}.$$  \hspace{1cm} (9)

The simulators use the speed dependent values of $R_{rot}$ and winding resistance $R$ given by (8) and (9), respectively.

### C. Experimental Results

The main objective of the testing was to show that the DMIC is capable of a CPSR of 6:1. To achieve this objective, dynamometer testing of the example motor was conducted at three speeds; the base speed of 400 rpm, 1215 rpm ($n = 3.04$), and 2424 rpm ($n = 6.06$). A detailed report on the experimental setup is contained in [10]. At each speed the advance angle was adjusted so that the motor current was close to the specified rated value of 212 A rms. The dynamometer used was a “water brake” type unit which can sustain a steady operating condition but is hard to adjust. Consequently, the experimenters took measurements whenever the motor current was within a few amperes of the specified rating.

The results of the laboratory test are contained in Table II, which shows the dc supply voltage, rotor rpm, advance angle, blanking angle, rms motor current, and useful output horsepower at the three speed conditions.

<table>
<thead>
<tr>
<th>$V_{dc}$ (volts)</th>
<th>$N$ (RPM)</th>
<th>$\theta_a / \theta_b$ (elec deg)</th>
<th>$I_{rms}$ (A)</th>
<th>$P_{out}$ (hp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>41.9</td>
<td>400 ($n = 1$)</td>
<td>31.1 / 60</td>
<td>212</td>
<td>7.5</td>
</tr>
<tr>
<td>41.9</td>
<td>1215 ($n = 3.04$)</td>
<td>49.9 / 20</td>
<td>214</td>
<td>9.27</td>
</tr>
<tr>
<td>41.9</td>
<td>2424 ($n = 6.06$)</td>
<td>46.4 / 20</td>
<td>206</td>
<td>8.12</td>
</tr>
</tbody>
</table>

The experimental data show that the CPSR of the test motor is greater than 6:1 since 8.12 hp is developed at 2424 rpm, relative speed of $n = 6.06$, compared with the 7.5 hp developed at the 400 rpm base speed where $n = 1$. Also note that the 9.27 hp developed at a relative speed of 3 is 24% more than the rated power. It is characteristic of the DMIC that greater power can be developed above base speed than at base speed. The amount of additional power depends heavily on the motor inductance.

A blanking angle of 20° was used in the high-speed runs instead of zero. This is done as a safety precaution against inadvertent commutation failures.

A. The experimental results are contained in Table II, which shows the dc supply voltage, rotor rpm, advance angle, blanking angle, rms motor current, and useful output horsepower at the three speed conditions.

The experimental data show that the CPSR of the test motor is greater than 6:1 since 8.12 hp is developed at 2424 rpm, relative speed of $n = 6.06$, compared with the 7.5 hp developed at the 400 rpm base speed where $n = 1$. Also note that the 9.27 hp developed at a relative speed of 3 is 24% more than the rated power. It is characteristic of the DMIC that greater power can be developed above base speed than at base speed. The amount of additional power depends heavily on the motor inductance.

For comparison, the MATLAB simulator was used to investigate the performance at the same speed/current conditions as in the laboratory experiments. The results are given in Table III.

Comparing Tables II and III shows that the simulated results agree favorably with the experimental measurements. This confirms that the treatment of inverter, skin effect, and rotational losses used by the simulator, as described previously, are accurate. The simulated current waveforms for the three speed conditions are shown in Fig. 11(b) and have the same wave shape, peak, and rms values as the experimental observations of Fig. 11(a).

Based on the experimental data, we concluded that the DMIC was able to drive the example motor over a CPSR greater than 6:1, but it is not clear how much greater. Concern for the speed
rating of the test motor precluded testing at higher speeds. However, the simulator has sufficient accuracy to further investigate the extent of the CPSR of the DMIC when driving the test motor.

The simulator was used to study the performance of the example motor over the entire speed range. Below base speed, the simulator uses hysteresis band current regulation. At base speed and above, the current regulator is ineffective and phase advance controls the motor current. The motor controls were adjusted to produce rated rms current for speeds from 50 rpm through 3200 rpm. The results of the simulations are shown in Fig. 12. The controls of the motor shown in the figure are the set point of the current regulator, \( I_{\text{set}} \), the advance angle, \( \theta_a \), denoted as “tha” in the figure, and the blanking angle, \( \theta_b \), denoted as “thb.” Below base speed, the phase advance is set to zero and the blanking angle is held at 60°. All control is done by adjustment of the current regulator set point, \( I_{\text{set}} \). The hysteresis band around \( I_{\text{set}} \) was ±5 A. As the speed approaches base speed, the current regulator begins to lose effectiveness and the regulator tries to compensate by increasing the set point. At the base speed, further increases in set point have no effect; in fact, without phase advance the current would begin decreasing no matter how large the current regulator set point might be. Above base speed, the advance regulator becomes active. We have found it convenient to ramp the blanking angle from 60 to 20° between base speed and 1.6 times base speed. As explained in [6], reducing the blanking angle increases the commutation time, which in turn, increases power conversion; however, control of the current magnitude and torque production is mainly through the advance angle, \( \theta_a \). The effectiveness of the controls is shown in Fig. 12 which indicates that the rms current was maintained at the rated value of 212 for each speed. The power versus speed capability is also displayed in Fig. 12. For comparison, the rated power of 7.5 hp is marked in the figure. Note that the power produced at rated current exceeds 7.5 hp for all speeds between 400 rpm and 3200 rpm. Thus, the simulator predicts that the CPSR for the example motor is 8:1.

The experimental data of Table II are overlaid on the simulated performance in Fig. 12. Experimental data points are marked with an “X.” There is reasonable agreement between simulated and experimental data, which indicates that the treatment of losses in the simulator is accurate and that the CPSR of the test motor is close to 8:1.

A CPSR of 6:1 is more than adequate for many applications. However, heavy-duty electric vehicles might require a CPSR in the range of 10:1. To achieve such a CPSR would require design for small speed-dependent losses.

IV. CONCLUSION

Laboratory testing has shown that the DMIC can drive a low-inductance BDCM over the wide CPSR required in electric vehicle applications. The CPSR of a test motor was experimentally shown to be greater than 6:1. Experimentation at speeds greater than six times base speed was precluded by the speed rating of the test motor rotor.

Key factors limiting the CPSR are the speed-dependent losses of the motor. These include hysteresis and eddy currents, friction and windage, and winding resistance increase caused by skin effect. Simulation, including speed-dependent motor losses, shows that the CPSR limit of the test motor is 8:1. The test motor was not designed for broad CPSR operation, and design changes to reduce speed dependent losses will increase the CPSR. For example, the stator laminations of the test motor are 14 mils thick and using a 5-mil lamination would reduce the core losses.

The proof-of-principle testing was sufficiently encouraging that a 20-hp BDCM has been designed and built for broad CPSR operation with the DMIC. This motor will be laboratory tested in the near future.

REFERENCES

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